

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit having nonvolatile memory cells each of which comprises one memory transistor, two switch transistors and two diffusion-layer lines, wherein said memory transistor includes a gate insulating film having discrete traps and a memory gate electrode connected to a word line, said two diffusion-layer lines constitute a source line and a bit line, and the switch gate electrodes of said two switch transistors are extended along said source line and said bit line.
2. A semiconductor integrated circuit according to claim 1, wherein said switch gate electrodes of said switch transistors which share said diffusion-layer lines are commonly connected.
3. A semiconductor integrated circuit according to claim 1, wherein each of said switch gate electrodes of said switch transistors has a width smaller than a technology feature size.
4. A semiconductor integrated circuit according to claim 1, comprising a control circuit for carrying out program by accelerating the carriers introduced from the channel of said switch transistors to the channel of said memory transistor and injecting the carriers to said gate insulating film having the discrete traps.
5. A semiconductor integrated circuit according to claim 1, wherein said gate insulating film having the discrete traps includes a silicon nitride film.

6. A semiconductor integrated circuit having nonvolatile memory cells each of which comprises one memory transistor, two switch transistors and two transistor inversion-layer lines, wherein said memory transistor includes a gate insulating film having discrete traps and a memory gate electrode connected to a word line, said two transistor inversion-layer lines constitute a source line and a bit line, and said two switch transistors and said two transistor inversion-layer lines constituting said source line and said bit line share said memory gate electrode, respectively.

7. A semiconductor integrated circuit according to claim 6, comprising a control circuit for carrying out program by accelerating the carriers introduced from the channel of said switch transistors to the channel of said memory transistor and injecting the carriers to said gate insulating film having the discrete traps.

8. A semiconductor integrated circuit according to claim 7, comprising a control circuit for carrying out erase by drawing out the carriers held by said gate insulating film having the discrete traps to said word line.

9. A semiconductor integrated circuit having nonvolatile memory cells each of which comprises one memory transistor, one switch transistor, one transistor inversion-layer line and one diffusion-layer line, wherein said one memory transistor includes a gate insulating film having discrete traps and a memory gate

electrode connected to a word line, said one transistor inversion-layer line constitutes a source line, said one diffusion-layer line constitutes a bit line, and said one switch transistor and said one transistor inversion-layer line constituting said source line share said memory gate electrode, respectively.

10. A semiconductor integrated circuit according to claim 9, comprising a control circuit for carrying out program by accelerating the carriers introduced from the channel of said switch transistor to the channel of said memory transistor and injecting the carriers to said gate insulating film having the discrete traps.

11. A semiconductor integrated circuit according to claim 10, comprising a control circuit for carrying out erase by drawing out the carriers held by said gate insulating film having the discrete traps to said word line.

12. A semiconductor integrated circuit having nonvolatile memory cells each of which comprises two memory transistors, one switch transistor and two diffusion-layer lines, wherein each of said memory transistors includes a gate insulating film having discrete traps and a memory gate electrode connected to a word line, said two diffusion-layer lines constitute a source line and a bit line, and the switch gate electrode of said one switch transistor is extended along said source line and said bit line.

13. A semiconductor integrated circuit according

to claim 12, wherein each of said memory gate electrodes of said memory transistors has a width smaller than a technology feature size.

14. A semiconductor integrated circuit according to claim 12, wherein said gate insulating film having the discrete traps includes a silicon nitride film.